Amendments to the Specification:

[0043] The present invention uses extended resonance which is a power dividing/combining technique, which has been exploited for the design of power amplifiers at microwave and millimeter wave frequencies. It results in very compact structures with high dividing/combining efficiency (>90%) up to millimeter wave frequencies. An N-port extended resonance dividing circuit is shown in FIG. 1. The admittance of the first and the last port is G+jB (where G is conductance and B is susceptance), whereas the admittance of the each interior port is G+2jB. The length of the transmission line, l_1, is chosen such that the admittance of the first port is transformed to its conjugate, G-jB. The admittance at the plane of the second port will be 2G+jB. As can be seen, half of the susceptance of the second device is cancelled in this process. The length of the ~~second~~ next transmission line ~~l_2~~ for port #2 (not shown in FIG. 1), is chosen to transform 2G+jB to its conjugate, 2G-jB (not shown in FIG. 1). ~~The admittance at the plane of the third port will be 3G+jB (not shown in FIG. 1).~~ This process is performed (N-1) times. At the last stage, the admittance at the plane of the $(N-1)^{th}$ transmission line, l_{N-1}, will be (N-1)G-jB transformed to its conjugate (N-1)G+jB and the admittance at the plane of the N^{th} port will be NG, which is matched to the source impedance Rs using a quarter-wave transformer, $\lambda/4$. Resonating all the ports with one another essentially places the ports in shunt, and analysis of this structure shows that the voltage at each port is equal in magnitude, but generally not in phase. This feature has been exploited for the design of power amplifiers at microwave and millimeter wave frequencies. It can be shown that by correct selection of susceptance B and conductance G, one can maintain equal power division, and vary the relative phase shift between device nodes by changing susceptance B. It should also be mentioned that it is possible to design an extended resonance dividing circuit for arbitrary imaginary part of the port admittances as long as the admittances are transformed to their conjugates and the last stage is matched to the source impedance Rs.

[0044] The concept of a phased array based on the extended resonance technique can be explained as follows: The port in FIG. 1 compared to FIG. 2 is modeled as a shunt combination of an antenna ($G=G_{ant}$) and a capacitor ($B=\omega C$). An inductor, ~~generally illustrated by the symbol L,~~ L_1, L_2 in FIG. 2, is used to transform the admittance to its conjugate instead of a transmission line, generally illustrated by ~~the symbol *l*,~~ l_1, etc. as used in FIG. 1. A schematic illustration of the proposed phased array is shown in FIG. 2. The antennas are assumed to be $\lambda/2$ apart, and the capacitors C and inductors ~~L~~ L_1, L_2, etc., are assumed to be tunable. It can be shown that the required inductance to transform the admittance, ~~$nG_{ant}+j\omega C$,~~ i.e. $2G_{ant}+j^{wc}$ to its conjugate, ~~$nG_{ant}-j\omega C$,~~ $2G_{ant}-j^{w\cdot C}$ is:

$$L_n = \frac{2C}{(nG_{ant})^2 + (\omega C)^2} \qquad (1)$$

[0048] To demonstrate the operation of this technique, a two GHz extended resonance based phased array including four edge coupled microstrip patch antennas placed half wavelength apart was designed, fabricated and tested. A 31 mil thick RT/DUROID™ 5880 high frequency laminate substrate from Rogers Corporation was used to build the phased array. MSV34 series chip varactor diodes from Metelics Inc. were used as tunable capacitors. A photo of the phased array can be seen in FIG. 7. The overall size of the phased array was 39 x 25 cm^2. The measured H-plane pattern of the phased array for various diode voltages is shown in FIG. 8 and the measured performance is summarized in Table 1. The results show that the phased array can scan the beam +/-13.5 degrees with the application of 2 V to 30 V reverse bias to the varactor diodes. The side lobe level was better than 7 dB. The gain of the phased array was measured to be 8.3 dB at 30 V reverse bias applied to the varactors. It can be seen from FIG. 8 that the gain at 2 V is 6.9 dB lower than the gain at 30 V. This is due to the low quality factor of the varactor diodes at this voltage ($Q_{2V}=22$, $Q_{30V}=121$ at 2 GHz), resulting in significant amount of RF power dissipation within the diode and change in the input impedance, which degrades the return loss.

It should be noted that any type of tunable capacitors, such as ferroelectric or MEMS based tunable capacitors, switched capacitors using PIN diodes or MEMS switches, which have been known to have lower loss, can be used to fabricate the phased array. In extended resonance based phased arrays, fewer number of devices are employed compared to a conventional phased array system, thereby reducing the cost.

TABLE 1

The measured performance of the phased array.

Diode Voltage (V)	Scan Angle (degrees)	Beamwidth (3dB), deg.	Side Lobe Level (dB)
2	18	26	-7
4	5	28	-13
8	0	26	-14
12	-2	25	-13
18	-5	26	-10
24	-8	27	-9
30	9	29	-7.5

[0050] The concept of extended resonance based phased arrays is shown in FIG. 2. The concept uses tunable capacitors C and tunable inductors ~~L~~ L_1, L_2, etc.. The admittance seen at the plane of the 1st port ($G_{ant}+j\omega C$) is transformed to its conjugate ($G_{ant}-j\omega C$) using the 1st inductor (L_1). Similarly, the admittance at the 2nd port ($2G_{ant}+2j\omega C$) is transformed to its conjugate using the 2nd inductor (L_2). This process is performed (N-1) times, and the admittance seen at the plane of the last port will be NG_{ant}, which is matched to the source impedance using a matching network. The analysis of this structure shows that the voltages at each port are equal in magnitude (equal power division among antennas), and the phase difference between adjacent ports are all equal to each other.

Therefore, by tuning the varactors as well as inductors, one can obtain equal power division among antennas and phase shifting between successive ports. Thus, a phased array system with one-dimensional scanning capability can be designed. Due to the initial phase offsets between the power divider ports, constant phase delays ($\Phi_{offset1}$, $\Phi_{offset2}$, . . . $\Phi_{offsetN}$) are used as shown in FIG. 2 to set the initial phases at the antenna nodes equal to each other. From then on, the beam is steered around the boreside of the antennas by tuning the varactors. It should also be noted that an extended resonance circuit can be designed for specified amplitude taper to achieve low side lobe. Since the magnitude of the voltage V is always the same as long as the admittances seen at the ports are transformed to their conjugates, non-uniform amplitude distribution can be obtained by adjusting the conductances seen at the ports (or antenna input impedances). In some designs unequal power distribution is desirable, for example arrays using Chebyshev tapered distribution for lower side lobes. The design according to the present invention can accommodate this.

[0059] A modified approach with improved performance is disclosed in the present invention. An N-port extended resonance power divider circuit is shown in Fig. 13. The admittance connected to the n port for n<N is G+2(n-1)jB, whereas the admittance connected to the last port is G+(N-1)jB. The length of the first transmission line, l_1, is chosen such that the admittance at the first port is transformed to its conjugate, G-jB. The admittance seen at the second port is 2(G+jB). Similarly, the length of the ~~second~~ next transmission line (not shown in FIG. 13), is chosen to transform 2(G+jB) to its conjugate, 2(G-jB) not shown in FIG. 13, ~~hence the admittance seen at the third port is 3(G+jB)~~. This process is performed (N-1) times, and at the last stage, the admittance seen at the plane of the $(N-1)^{th}$ transmission line will be (N-1)(G-jB) and the admittance seen at the N^{th} port will be NG, which is matched to the source impedance using a quarter-wave transformer. The analysis of this structure shows that the voltages at each port are equal in magnitude (equal power division), but not in phase. This feature has been exploited for the design of power amplifiers at microwave and millimeter wave frequencies.

[0065] Extended resonance beam-steering technique can also be used to design phased arrays with two dimensional scanning capability as shown in FIG. 21. Multiple 1-dimensional horizontal scanning arrays, similar to the array shown in Fig. 15, are fed using a vertically scanning extended resonance circuit to achieve 2-dimensional beam-steering capability.

[0066] To demonstrate the utility of this technique, a 2 GHz extended resonance based phased array consisting of four edge coupled microstrip patch antennas placed half wavelength apart was designed, fabricated and tested. A 31 mil thick RT/DUROID™ 5880 high frequency laminate substrate from Rogers Corporation and MSV34 series chip varactor diodes from Metelics Inc. were used to fabricate the phased array. The antenna dimensions were 2.31 x 1.96 inch^2. The input impedance of the antenna was designed as 67 Ω by recessing the feed point by 637 mils. The tunability of the varactors was 3.2:1 with the application of 3 V to 30 V reverse bias. A photo of the phased array is shown in FIG. 22. The overall size of the phased array is 15.4 x 9.8 inch^2. The radiation pattern of the phased array has been measured in an anechoic chamber, and the efficiency of its extended resonance feed was determined by measuring the magnitude and phase of the signal at each antenna node using a vector network analyzer. The measured scan angle and array feed efficiency versus the diode voltage is shown in FIG. 23. Measured H-plane patterns of the phased array for various diode voltages are also shown in FIG. 24 and the measured performance is summarized in

TABLE II

THE MEASURED PERFORMANCE OF THE PHASED ARRAY

Diode Voltage, V	Scan Angle, degrees	3 dB Beamwidth, degrees	Side Lobe Level, dB	Gain, dB	Efficiency, %
3	10	24	-91.	6.9	59
4	6	24	-12	7.5	67
8	2	26	-14	8.1	80
10	0	24	-13.5	8.4	82
12	-2	24	-12.5	8.4	82
18	-4	26	-11	8.6	83
24	-6	26	-11	8.7	82
30	-10	28	-9	8.7	80

[0069] FIG. 26 is a detailed illustration of an embodiment where a second tunable element is a switching fixed capacitor ~~C~~ C_1, C_s, C_3, C_n configuration to be inserted in place of the second tunable element illustrated in any of FIGS 1-3 or FIGS 13-15.

[0070] FIG. 27 is a detailed illustration of an embodiment where a second tunable element is a switching transmission line ~~l~~ l_1, l_2, l_n configuration to be inserted in place of the second tunable element illustrated in any of FIGS 1-3 or FIGS 13-15.